

**National University**



of Computer

and

Emerging Sciences

Chiniot

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Faisalabad Campus



**EE1005 – Digital Logic Design**

**Quiz# 3**

**Instructor:** Muhammad Adeel Tahir **Section:** CS-2F **Time:** 20 Minutes

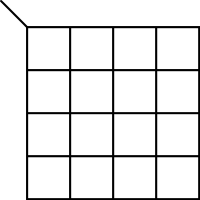
**Name: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_**

**Roll No: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ Total: 20 marks**

**Note:** Use the back side of the page if needed. Make sure the handwriting is neat while drawing the circuit, quiz will be marked as 0 if attempted in a writing that is not readable at all. **Cutting will lead to negative marking.**

**Q1: Implement the following Boolean function F together with the don't-care condition d using no more than two NOR gates. Assume that both the normal and complement inputs are available. (Show proper grouping) (10 marks)**

**Circuit Diagram:**



**F = \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_**

**Q2: Implement the following Functions as 2-level NAND only circuits:**

1. **(2.5+2.5 = 5 marks)**
2. **(2.5+2.5 = 5 marks)**

(Note: Show working in both, in case of a mistake in complement sign it shall be marked as 0 without any partial marks)

a)